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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,599	02/06/2002	Ricky Merle Peterson	ROC920010319US1	8298

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IBM INTELLECTUAL PROPERTY LAW DEPARTMENT  
DEPARTMENT 917, BUILDING 006-1  
3605 HIGHWAY 52 NORTH  
ROCHESTER, MN 55901-7829

EXAMINER
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SHAH, NILESH R

ART UNIT	PAPER NUMBER
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2195

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/068,599

Applicant(s)

PETERSON, RICKY MERLE

Examiner

Nilesh Shah

Art Unit

2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Claims 1-11 are presented for examination.

#### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:  
  
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chastain et al (5,050,070) (hereinafter Chastain) in view of Brenner et al (6,658,449) (hereinafter Brenner).
4. As per claim 1, Chastain teaches in the invention substantially including an apparatus comprising:  
  
a plurality of processors, each processor having the capability of executing a plurality of threads(col. 3 lines 25-28);  
  
a memory coupled to the plurality of processors(col. 4 lines 17-31); and

a thread dispatch mechanism residing in the memory and executed by at least one of the plurality of processors(col. 6 lines 46-52; col. 5 lines 44-50;col.17 1-39).

Chastain does not specifically teach the use of determining an idle thread.

Brenner teaches the thread dispatch mechanism determining which of the plurality of processors are idle(col. 4 lines 47-50), which of the plurality of processors can accept an additional thread(col. 4 lines 54-56), and which of the plurality of processors cannot accept an additional thread(col. 5 lines 37-45; col. 10 lines 49-65), the thread dispatch mechanism dispatching a new thread to an idle processor, if one exists (col. 4 lines 54-56;col. 25-40).

It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Brenner and Chastain because Brenner's method of determining which processor is idle would improve Chastain's system by allowing each processor to execute threads in a high throughput manner.

5. As per claim 2, Brenner teaches an apparatus wherein, if none of the plurality of processors is idle and if at least one of the plurality of processors can accept an additional thread, the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept an additional thread (col. 4 lines 46-56; col. 5 lines 37-45; col. 10 lines 49-65).
6. As per claim 3, Brenner teaches an apparatus wherein, if all of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism waits for one of the

plurality of processors to complete processing a thread, thereby becoming a processor that can accept an additional thread, and then dispatches the thread to the processor that can accept an additional thread (col. 5 lines 37-45; col. 10 lines 49-65).

7. As per claim 4, Chastain teaches a method for dispatching threads in a computer system that includes a plurality of processors that can each execute a plurality of threads, the method comprising the steps of: determining the status of each of the plurality of processors (col. 6 lines 46-52; col. 5 lines 44-50; col. 17 1-39).

Brenner teaches wherein a processor is idle if not executing any threads, wherein the processor can accept an additional thread if busy working on one or more threads but has the capacity to process the additional thread (col. 4 lines 46-56; col. 5 lines 37-45; col. 10 lines 49-65), and wherein the processor cannot accept an additional thread if busy working on a maximum number of threads the processor can execute (col. 4 lines 47-50) and dispatching a new thread to an idle processor, if one exists (col. 5 lines 37-45; col. 10 lines 49-65).

8. Claims 5-6 are rejected based on the same rejection as claims 2-3 above.
9. As per claim 7, Chastain teaches a program product comprising:  
computer-readable signal bearing media bearing the thread dispatch mechanism (col. 4 lines 17-66).

the plurality of processors cannot accept an additional thread, the thread dispatch mechanism dispatching a new thread to an idle processor(col. 6 lines 11-15; col. 10 lines 43-66; col. 5 lines 45-60).

Brenner teaches

a thread dispatch mechanism that determines which of a plurality of processors in a multiprocessor computer system are idle, which of the plurality of processors can accept an additional thread(col. 4 lines 54-56), and if one exists, wherein each processor can execute a plurality of threads (col. 5 lines 37-45; col. 10 lines 49-65).

10. As per claim 8, Chastain teaches a program product wherein the computer-readable signal bearing media comprises recordable media (col. 4 lines 17-66).
11. Claim 9 is rejected based on the same rejection as claim 8 above.
12. Claims 10-11 are rejected based on the same rejection as claims 2-3 above.

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hardwick (6,292,822) teaches the use of plurality of processors and threads (col.38 lines 22-44) and if an idle processor is found then assign a thread to that processor (col. 4 lines 24-67)

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14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah  
Examiner  
Art Unit 2195

NS  
May 9, 2005



**MENG-AL T. AN**  
**SUPERVISORY PATENT EXAMINER**  
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